in a train of zeros as the high level of the signal varies from 100-mV to 500-mV above the reference voltage and the low level is held at its nominal value of 0-V.

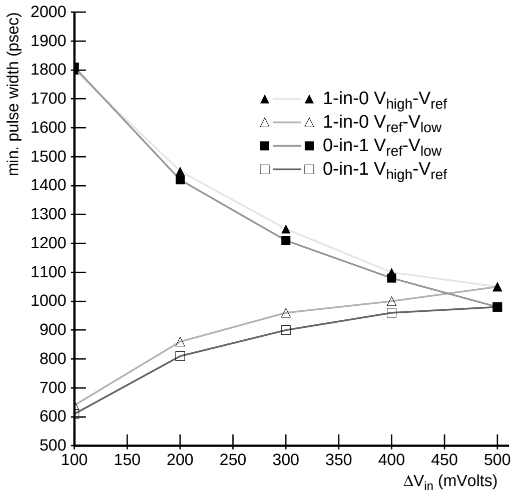

Figure 10. Detectable pulse width versus dc signal levels.

Figure 11 is an oscillograph of the receiver's output and the output of a differential amplifier [2] driven by the same input signals when a 350-MHz 300-mV sinusoidal signal is superimposed on the reference voltage. The differential amplifier receiver translates the noise on the reference line to an output phase noise of 1 ns peak-to-peak making reception of the signal impossible with the techniques described in [2]. The output of the current integrating receiver did not show any failure and experiences minimal jitter (< 150ps peak-to-peak).

Conclusion

A robust high speed sampler for fast system interfaces has been proposed. The sampler utilizes current integration to filter out high frequency noise. A prototype receiver design has been fabricated in a 1.2 μm CMOS technology.

The receiver pair operates at a data rate of 500 Mbps/pin and shows improved noise immunity compared to a previous design [2]. Applications of this design include high bandwidth memory interfaces and multiprocessor interconnection networks.

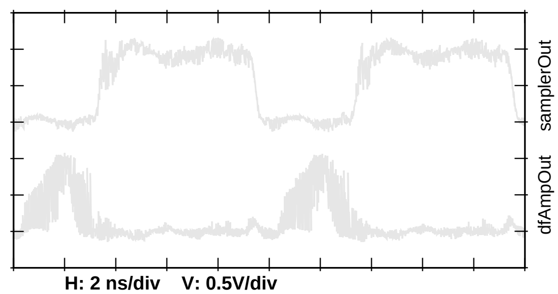

Figure 11. Waveforms in the presence of reference noise.

Acknowledgments

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References

[1] N. Kushiyama, S. Oshima, D. Stark, H. Sakurai, S.Takase, T. Furuyama, T. Barth, A. Chan, J. Dillon, J. Gasbarro, M. Griffin, M. Horowitz, ''500 Mbyte/sec Data-Rate 512 KBits x 9 DRAM Using a Novel I/O Interface'', in *IEEE JSSC, vol. 28, No. 4.* April 1993.

[2] S. Sidiropoulos, K. Yang, M. Horowitz, ''A CMOS 500 Mbps/pin point-to-point link interface'', in *1994 Symposium on VLSI Circuits Digest of Technical Papers*, June 1994.

[3] B. Gunning, L. Yuan, T. Nguyen, T. Wong, ''A CMOS Low Voltage-Swing Transmission-Line Transceiver'', in *1992 ISSCC Digest of Technical Papers*, February 1992.

[4] A. Yukawa, ''A CMOS 8-bit High-Speed A/D Converter IC''. in *IEEE JSSC, vol. 20, No. 3.*, June 1985.

network from the latch kick-back and also level-shifts the low common mode of the integrator differential output to improve the latch performance.

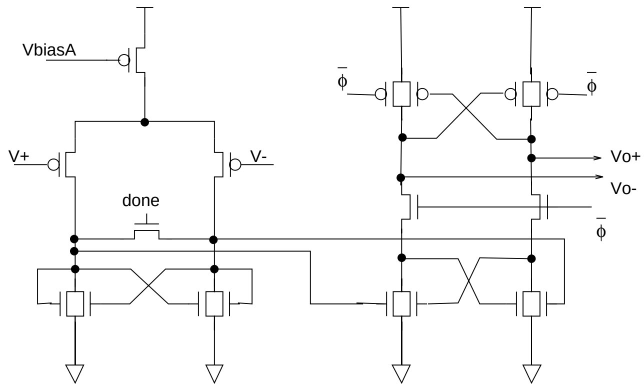

Figure 7. Amplifier and latch schematic.

The amplifier uses a combination of cross coupled and diode connected loads which form a high differential impedance for increased small signal gain. At the same time, the diode clamps limit the output swing, facilitating faster reset and reducing kick-back. The differential latch [4] converts the low swing output of the amplifier to a full swing CMOS signal. The output of this precharged latch is held stable for a full clock period by using a simple cross coupled NOR latch structure (not shown in Figure 7). Figure 8 shows simulated waveforms of the circuit operating at a clock frequency of 250 MHz.

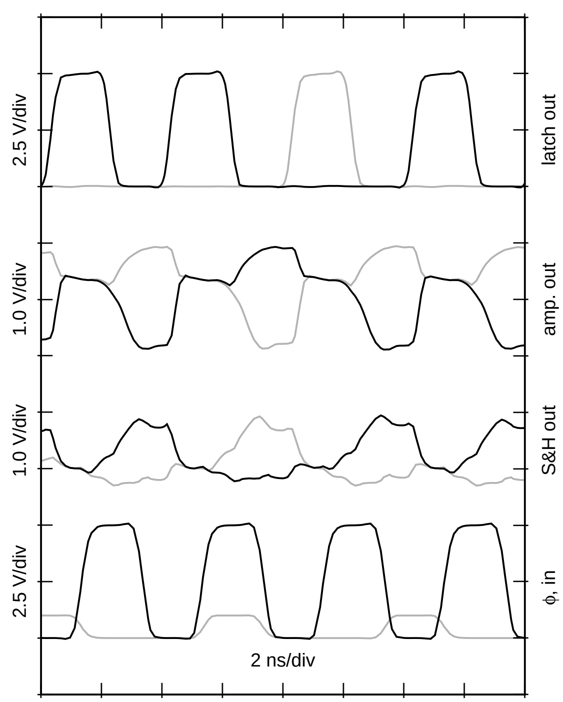

Figure 8. Simulated receiver operation.

The deviations of the behavior of this integrating receiver from the ideal depend on the systematic and random offsets of the design. These deviations will cause a shift of the center of the sampling uncertainty window and decrease the maximum skew tolerance of the receiver. This would be seen as a shift of the zero crossing on the time axis in Figure 3. Systematic offsets are mainly introduced by mismatch in the ratio between the gate and drain capacitance in the tail boosting circuit and the delay of the sample and hold network (Fig. 5). These systematic offsets can be partly cancelled if the DLL used to position the sampling clock utilizes a replica of the receiver as its phase detector. On the other hand random offsets (i.e. mismatches between nominally identical devices) cannot be cancelled

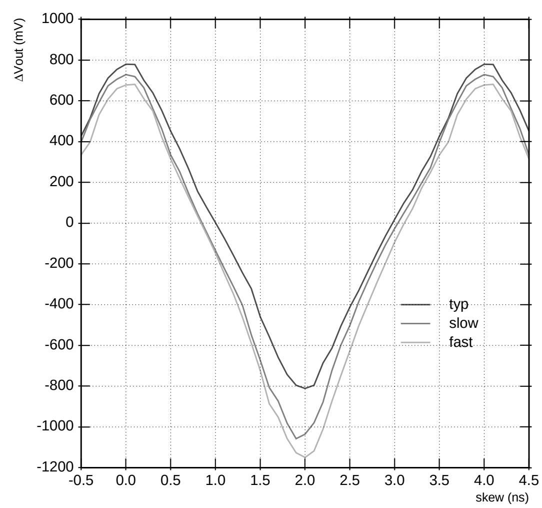

Figure 9. Simulated integrator characteristics.

Simulation results indicate that the maximum time shift that can be caused by a 20-mV threshold mismatch and 5% width variation in the first stage is less than 100 psec. Figure 9 shows the simulated behavior of the integrator in the presence of skew over various process and environmental condition corners, operating at a frequency of 250 MHz. Figure 9 indicates that the maximum time shift of the zero crossing point due to systematic offsets over various process corners is 180 psec (i.e 9% of the 2 nsec bit valid-time).

Experimental Results

A prototype receiver design has been fabricated in the HP CMOS34 1.2 μm process, using the MOSIS scalable CMOS design rules. This test chip contains four prototype receivers, their associated biasing circuits, clock buffers with controllable delay, and monitoring circuits which allow the determination of the phase relationship between the internal sampling clock and the incoming data signal. Each of the receivers dissipates 2.7 mW of power and occupies 60 x 450 μm^2 of silicon area.

Operating from a 5-Volt supply, the chip functions up to a 300 MHz clock rate (i.e. 600 Mbps/pin transfer rate). Measurements performed at the target operating frequency of 250 MHz across different chips indicate that the sampling uncertainty window has a width of 150 psec and its center is located 850 ps from the positive clock edge (i.e. a systematic offset of 150 ps is present in this process run).

Figure 10 shows the minimum detectable pulse width as a function of the input levels – for example, curve "1-in-0 V_{high}-V_{ref}" shows the minimum detectable width of a single high pulse

The block diagram of an MOS implementation of the current integrating receiver is shown in Fig. 4(a). In this implementation the input signals switch between 0 and 1 Volts and are compared against a 500-mV reference voltage [2], or they can be compatible with the levels of the GTL interface [3]. The receiver consists of an MOS current integrating stage, followed by a sample and hold circuit, an amplifier and a differential latch. Two receivers are used in parallel to sample the data transmitted on both of the clock half-periods, therefore doubling the effective transfer rate.

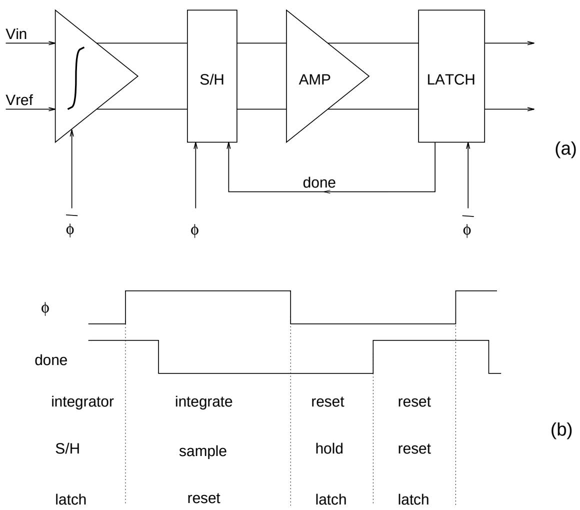

Figure 4. Block diagram (a) and operation (b) of the receiver.

The timing for the receiver is shown in Fig. 4(b). During the sampling period, the differential output voltage of the first stage is sampled and amplified while the latch is being reset. When phase ϕ goes low the sample and hold network enters the hold state and the first stage is reset. Subsequently, the latch is triggered by a slightly delayed version of ϕ's falling edge in order to compensate for the delay of the amplifier. When the output of the latch has settled, the sample and hold network is reset. This self-timed reset facilitates equalization of all the intermediate nodes in the circuit, thus eliminating data dependent systematic offsets.

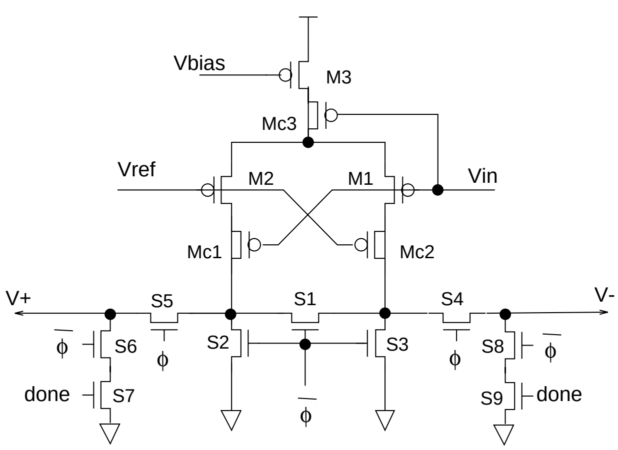

Figure 5. First stage schematic.

The schematic diagram of the current integrator and the sample and hold stage is shown in Figure 5. Transistors M_1-M_3 form the integrating current switch. Transistors S_1-S_3 are the integrator reset switches, and S_4-S_9 are the differential sample and hold network. In order to accomplish complete current steering in the switch with only a fraction of the maximum differential voltage present at the input (i.e. operation close to that of an ideal integrator), devices M_1 and M_2 are made fairly wide (120 µm for 200 µA of tail current for 250 MHz operation). This results in a significant parasitic drain capacitance at the output of the integrator and as a consequence no explicit load capacitance is incorporated in this design – the differential pair integrates its current on its own parasitics. A systematic offset is introduced into the integrator because of the coupling that is introduced on to the output node by the gate overlap capacitor of M_1. Transistors M_{c1}, M_{c2} cancel this systematic offset. These two devices have a size of 1/2 the input devices and they always remain off, making the gate overlap coupling of M_1 common mode. Since the input of the current switch is single ended, the tail node must first settle at a gate overdrive above V_{in} or V_{ref} (depending on which one is lower), before the tail current will be steered to one of the branches. The significant junction capacitance of the tail node makes this settling slow and therefore introduces another systematic offset into the integrator. Device M_{c3} cancels this offset by boosting the tail node when the input transitions.

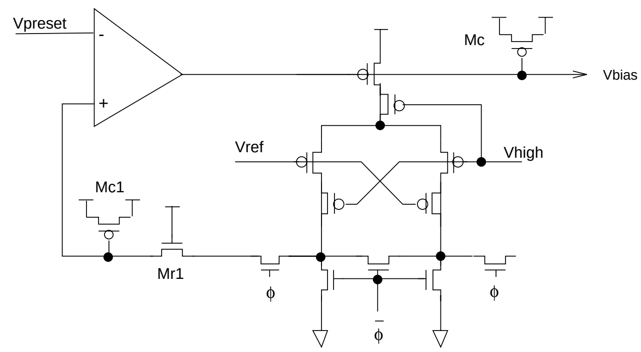

Figure 6. Replica feedback bias circuit schematic.

Using parasitic drain capacitance as the integrating capacitor makes the output swing of the first stage sensitive to process variations. In order to compensate for process skews and also adjust the integration current as a function of the operating clock frequency, the first stage of all the receivers is biased by the circuit shown in Figure 6. This replica bias circuit dynamically adjusts the current through the PMOS current source so that the integrator output swing is held constant and independent of the value of the parasitic capacitor and the operating clock frequency. This circuit functions as follows. The output of an integrator replica is low pass filtered through M_{r1}-M_{c1} and subsequently fed to an operational amplifier which compares it with a preset voltage. The operational amplifier dynamically adjusts the current through the integrator replica so that the low-pass filtered output remains equal to the preset voltage. Compensation for the bias circuit is accomplished with an explicit compensation capacitor formed by M_c.

Figure 7 shows the schematic diagram of the amplifier and the latch. The amplifier buffers the output of the sample and hold

Current Integrating Receivers for High Speed System Interconnects*

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ABSTRACT

This paper presents a high speed receiver design that utilizes current integration in order to increase its noise immunity. The integration of current on a capacitor based on the incoming signal voltage effectively averages the incoming signal over its valid time period, therefore filtering out high frequency noise. An experimental design illustrating the concept has been fabricated in a 1.2 μm CMOS technology. The receiver dissipates 2.7 mWatts of power operating from a 5-Volt supply, achieves error free operation at a clock frequency of 250 MHz, and occupies 60 x 450 μm^2 of silicon area.

Introduction

High speed system interfaces [1], [2] usually transmit a high speed clock synchronously with a parallel data stream. The receiver utilizes a Phase or Delay Locked Loop to position the sampling clock edge in the middle of the incoming data eye and uses both the clock edges to sample the incoming data (Fig. 1). Although phase shifting the clock by 90^o provides maximum set-up and hold times for the input sampler, this scheme is still prone to erroneous reception due to the fact that only one sample of the data is taken per incoming bit period – reflection or switching noise occurring during the sampling edge may cause the sampler to receive the wrong bit value.

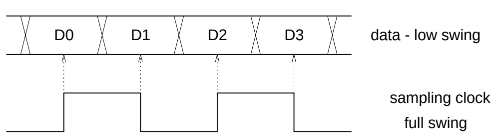

Figure 1. Timing of high speed interface signals.

A solution to the above problem would be to increase the number of samples taken per bit period and use a majority voting scheme to determine the value of the transmitted data. The disadvantages of such a solution are that the required power and area increase linearly with the number of samples. Additionally positioning the sampling edges precisely may become difficult at high speeds. The alternative we chose is the analog equivalent of majority voting, i.e. integrate current on a capacitor and then decide at the end of the sampling period on the polarity of the incoming data. Such a scheme would require only a single clock defining the sampling/integration period and its power and area requirements are moderate.

Receiver Design

Figure 2 shows the schematic of an ideal current integrator. It consists of an ideal current switch, a pair of integrating capacitors, and two reset switches. The level of clock phase φ indicates the input data-valid period. When φ is low the switches are closed, resetting the integrator. When φ is high current is steered to the branches of the switch and dumped on the capacitors depending on the input voltage. At the end of clock phase φ the polarity of the output differential voltage ΔV indicates whether the input signal was mostly low or high during the integrating period. The behavior of this ideal integrator in the presence of skew between the input signal and the sampling clock phase is illustrated in Figure 3.

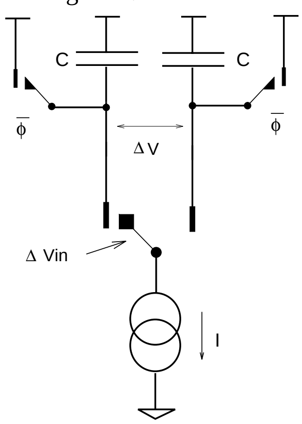

Figure 2. Ideal Current Integrator.

The differential output voltage ΔV reaches its maximum or minimum value of $\pm(I \times T)/(2 \times C)$ when the input signal and the sampling clock are in phase or 180^o out of phase (where I is the switch current, T is the clock period, and C the integrating capacitor size). The differential output voltage is zero when the input signal and the sampling clock are in quadrature.

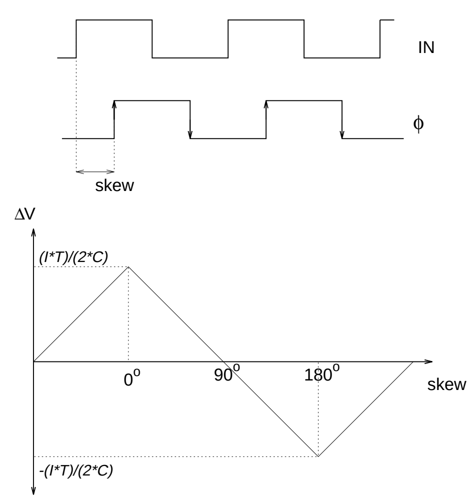

Figure 3. Ideal integrator characteristics.

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